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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/729,544

12/05/2003

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09/01/2010

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EXAMINER

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ART UNIT

PAPER NUMBER

2826

MAIL DATE

DELIVERY MODE

09/01/2010

PAPER

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte NICHOLAS R. WATTS, ERIC C. PALMER, JUI MIN LIM,
TODD B. MYERS, and BOONSRI WANGMANEERAT

Appeal 2009-004158
Application 10/729,544¹
Technology Center 2800

Before JOSEPH F. RUGGIERO, MARC S. HOFF, and
THOMAS S. HAHN, *Administrative Patent Judges*.

HOFF, *Administrative Patent Judge*.

DECISION ON APPEAL²

¹ The real party in interest is Intel Corporation.

² The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, or filing a request for rehearing, as recited in 37 C.F.R. § 41.52, begins to run from the “MAIL DATE” (paper delivery mode) or the “NOTIFICATION DATE” (electronic delivery mode) shown on the PTOL-90A cover letter attached to this decision.

STATEMENT OF CASE

Appellants appeals under 35 U.S.C. § 134 from a Final Rejection of claims 15, 17-19, 21, 22, 34, 36, 37, and 39-43.³ We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

Appellants' invention concerns a stacked integrated circuit (IC) package. Each layer ("package component") includes a substrate 12, with a metal layer on the top surface and bottom surface of the substrate. Metal layer 20 formed on the bottom surface of the substrate may include a ground plane 28 and pads 30 by which connection may be made to another IC package component or to electronic components outside the stacked IC package. The substrate may also include metallized vias 32 to provide connections between metal layers 18 and 20 (Spec. 3).

Claims 15 and 40 are exemplary of the claims on appeal:

15. An article of manufacture, comprising:

at least two integrated circuit (IC) packages in stacked relation to each other, each of IC packages including:

a substrate;

an IC mounted on a first surface of the substrate;

a ground plane formed on an opposite surface of the substrate from the first surface on which the IC is mounted; and

³ Claims 1-14, 16, 20, 23-33, 35, and 38 have been canceled.

a coverlay formed of an organic material and laminated on the first surface of substrate and having at least one opening formed by photolithography; and

at least one conductive connection formed through one of the coverlays and connecting one of the ICs to another of the ICs;

wherein each IC is positioned in an opening of a respective one of the coverlays, the opening formed by photolithography, all of said each IC being in said opening of said respective one of the coverlays.

40. The article of manufacture of claim 15, further comprising:
a solder mask layer which covers the ground plane.

The Examiner relies upon the following prior art in rejecting the claims on appeal:

Sota	US 6,201,707 B1	Mar. 13, 2001
Blumenau	US 6,421,711 B1	July 16, 2002
Rokugawa	US 6,441,314 B2	Aug. 27, 2002
Murayama	US 6,548,330 B1	Apr. 15, 2003

Claims 15, 17, 18, 34, and 36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Murayama in view of Sota.

Claims 19, 21, 22, 37, and 39 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Murayama in view of Sota and Blumenau.

Claims 40 and 42 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Murayama in view of Sota and Rokugawa.

Claims 41 and 43 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Murayama in view of Sota, Blumenau, and Rokugawa.

Throughout this decision, we make reference to the Appeal Brief (“App. Br.,” filed Nov. 22, 2006), the Reply Brief (“Reply Br.,” filed

May 17, 2007) and the Examiner's Answer ("Ans.," mailed Mar. 21, 2007) for their respective details.

ISSUES

With respect to claim 15, Appellants argue that interconnection pad 6 of Murayama cannot correspond to the claimed ground plane because (a) one of ordinary skill in the art would clearly understand "ground plane" to refer to a metal layer of considerable extent, positioned to serve as ground for an integrated circuit (App. Br. 11); (b) Murayama's interconnection pad is of very limited extent and much too small to be characterized as a plane (App. Br. 11); and (c) interconnection pad 6 is located so as to provide interconnection between one integrated circuit and another, and as such is completely unsuitable to serve as ground (App. Br. 11).

With respect to claim 40, Appellants further argue that the proposed modification of Murayama and Sota in view of Rokugawa would render the modified structure unsuitable for its intended purpose, because covering interconnection pad 6 with a solder mask would cause it to be insulated from below, and thus unable to provide signal connection to a lower level of the stacked IC structure (App. Br. 12).

Appellants' contentions present us with the following issues:

1. Does interconnection pad 6 of Murayama correspond to the "ground plane" recited in the claims, as the term is understood by the person having ordinary skill in the art?
2. Would the Examiner's proposed modification of Murayama in view of Sota and Rokugawa render the modified structure unsuitable for its intended purpose?

FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

Murayama

1. Murayama teaches a “back interconnection” pad 6 formed on the lower side of substrate 2 (col. 4, l. 18, 52-53; Fig. 1).

PRINCIPLES OF LAW

On the issue of obviousness, the Supreme Court has stated that “the obviousness analysis cannot be confined by a formalistic conception of the words teaching, suggestion, and motivation.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 419 (2007). Further, the Court stated “[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.” *Id.* at 416. “One of the ways in which a patent’s subject matter can be proved obvious is by noting that there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent’s claims.” *Id.* at 419-420.

ANALYSIS

CLAIMS 15, 17-19, 21, 22, 34, 36, 37, AND 39

We select claim 15 as representative of this group of claims, pursuant to our authority under 37 C.F.R. § 41.37(c)(1)(vii).⁴

⁴ Appellants indicate that their arguments with respect to the § 103 rejection of claims 15, 17, 18, 34, and 36 over Murayama in view of Sota are also applicable to the § 103 rejection of claims 19, 21, 22, 37, and 39 over Murayama in view of Sota and Blumenau (App. Br. 8).

Appellants' argument that interconnection pad 6 of Murayama cannot correspond to the claimed "'ground plane'" is not persuasive (*see* FF 1). Appellants provide no evidence to support their allegation that one of ordinary skill in the art would clearly understand a "'ground plane'" to be "a metal layer of considerable extent" (App. Br. 11). Because of this lack of evidence, Appellants have not established that the "extent" of Murayama's connection pad is insufficiently "considerable."

The Examiner finds, and we agree, that the term "'ground plane'" does not imply a specific size, nor a specific structure (other than being planar) (Ans. 8), and further finds that the size of interconnection pad 6 does not prevent it from being a plane (Ans. 9). We agree with the Examiner's further finding that interconnection pad 6 is capable of working as a ground plane because it can be connected to ground voltage (Ans. 8-9).

Last, Appellants' argument that interconnection pad 6 is located so as to provide interconnection between one IC and another and is thus unsuitable to serve as a ground is similarly unpersuasive (App. Br. 11). The Examiner finds, and we agree, that the fact that some interconnections may be commonly connected to ground does not imply that other interconnections cannot be connected to power or signal voltages (Ans. 9).

Appellants have not established that the Examiner erred in rejecting representative claim 15. Accordingly, we will sustain the Examiner's § 103 rejection of claims 15, 17, 18, 34, and 36 over Murayama in view of Soto, and we will sustain the Examiner's § 103 rejection of claims 19, 21, 22, 37, and 39 over Murayama in view of Sota and Blumenau.

CLAIMS 40-43

We select claim 40 as representative of this group of claims, pursuant to our authority under 37 C.F.R. § 41.37(c)(1)(vii).⁵

Appellants' further argument (summarized *supra*) with respect to claim 40 is not persuasive to show Examiner error. We agree with the Examiner that the proposed combination of references would not require that the entire ground plane be covered by a solder mask layer, but rather only the exposed areas of the ground plane to protect them from corrosion (Ans. 9). Consequently, we do not agree with Appellants that the proposed modification would render the modified structure unsuitable for its intended purpose. We will therefore sustain the Examiner's § 103 rejection of claims 40 and 42 over Murayama in view of Sota and Rokugawa, and we will sustain the Examiner's § 103 rejection of claims 41 and 43 over Murayama in view of Sota, Blumenau, and Rokugawa.

CONCLUSION

1. Interconnection pad 6 of Murayama corresponds to the "ground plane" recited in the claims, as the term is understood by the person having ordinary skill in the art.

2. The Examiner's proposed modification of Murayama in view of Sota and Rokugawa would not render the modified structure unsuitable for its intended purpose.

⁵ Appellants indicate that their arguments with respect to the § 103 rejection of claims 40 and 42 over Murayama in view of Sota and Rokugawa are also applicable to the § 103 rejection of claims 41 and 43 over Murayama in view of Sota, Blumenau, and Rokugawa (App. Br. 8).

Appeal 2009-004158
Application 10/729,544

ORDER

The Examiner's rejection of claims 15, 17-19, 21, 22, 34, 36, 37, and 39-43 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(v).

AFFIRMED

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